

App. Serial No. 10/511,212  
Docket No. GB 020048US

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Remarks

The Office Action dated January 17, 2007 indicated an objection to the drawings and listed the following rejections: claim 15 stands rejected under 35 U.S.C. § 112(1) with regard to the written description; claims 1-9 and 11-14 stand rejected under 35 U.S.C. § 103(a) over Darwish *et al.* (U.S. 5,688,725) in view of Kocon *et al.* (U.S. 6,351,009); and claim 10 stands rejected under 35 U.S.C. § 103(a) over Darwish in view of Kocon, and further in view of Mo (U.S. 6,316,806).

Regarding the objection to the drawings, Applicant submits that the drawings are in compliance with 37 C.F.R. § 1.83(a), because the drawings properly convey to one skilled in the art every feature of the claimed invention. Applicant appreciates the Examiner's clarification for the rationale behind the objection; however, Applicant respectfully traverses the objections because the Examiner is erroneously reading limitations of claim 15 which do not exist. More specifically, the Examiner is erroneously asserting that two immediately adjacent regions are limited to the two immediately adjacent regions that are closer than any other two immediately adjacent regions. Applicant submits that such limitations are simply not present in the claim. More specifically, Applicant notes that starting at the second from the left ruggedness region 15 shown at the bottom of FIG. 2 three pairs of immediately adjacent ruggedness regions 15 are shown. For example, from the selected ruggedness region, an immediately adjacent ruggedness region exists in a left direction, a different immediately adjacent ruggedness region exist in a right direction and yet another immediately adjacent ruggedness region exist in an upward direction (*i.e.*, from the bottom of the page to the top of the page). Put another way, the Examiner's objection erroneously ignores immediately adjacent regions shown in the figures that are consistent with the claimed limitations. For example, Applicant notes that FIG. 2 shows immediately adjacent ruggedness regions in the bottom to top direction that are greater than two immediately adjacent source regions from the same bottom to top direction. Accordingly, because the Examiner's erroneous interpretation fails to consider these adjacent regions, the objection is improper. However, in an effort to facilitate prosecution, Applicant has amended claim 15. Applicant submits that the amendment is not for the purposes of overcoming any

App. Serial No. 10/511,212  
Docket No. GB 020048US

objections and is not intended to narrow the scope of the claimed limitations. Therefore, Applicant requests that the objection be removed.

Applicant traverses the Section 112(1) rejection of claim 15 because the subject matter of claim 15 is sufficiently described in the Specification. As indicated by the Examiner, the claimed subject matter must be described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For example, with reference to Applicant's Specification at Fig. 2 and paragraph 0033, the distance between adjacent ruggedness regions 15 (with an approximate length of about 1  $\mu\text{m}$ ) is greater than the distance between adjacent source regions 13 (with an approximate length of about 20  $\mu\text{m}$ ). Moreover, consistent with the claim amendments, Applicant submits that the length of the ruggedness regions 15 is less than the length of the source regions 13. Thus, the Section 112(1) rejection is improper and Applicant requests that it be withdrawn.

Applicant traverses the Section 103(a) rejection of claims 1-14, because the rejection is indiscernible and unsupported by any evidence that the prior art would lead the skilled artisan to implement anything similar to the proposed modification (as characterized by the Examiner). More specifically, the asserted combination would render the MOSFET device of the Darwish reference inoperable. Applicant submits that the proposed modification is illogical because the Examiner appears to have overlooked fundamental differences in the teachings of the asserted references. As stated by Applicant in the previous response, the Darwish reference states, in the few lines immediately before and after the "Summary of the Invention" (Darwish at Col. 3: 46-58), the purpose of Darwish is to employ the body region and heavily-doped (deep central P+ region) delta layer, *inter alia*, to provide a MOSFET with low on resistance. By using Kocon's source/body regions (306/304 of Fig. 3C) in between the trench gates (102/104 of Fig. 11G) of Darwish, the ensuing (hypothetical) Darwish embodiment would no longer have the P+ contact region 114 and P-body region 116 upon which the Examiner relies. Accordingly, the relied-upon embodiment of Darwish would not operate as intended. As consistent with relevant case law and the M.P.E.P., there is no motivation to modify a reference where the modification would undermine or defeat the purpose of the reference (*see, e.g., In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

App. Serial No. 10/511,212  
Docket No. GB 020048US

Because the proposed modification would undermine and defeat the purpose of Darwish, the rejection is improper and must be withdrawn.

The Examiner's response to Applicant's above argument appeared to rely upon a comparison between FIG. 4 and FIG. 3 (of the Kocon reference) purporting to show minimization of size between the two figures. Such a comparison is irrelevant to the fundamental differences between the asserted references as it merely shows improvement in the context of the Kocon reference. In an effort to clarify this fundamental difference to the Examiner, Applicant notes that the relied upon portion of Darwish (*i.e.*, FIG. 4) teaches a MOSFET that is configured such that the following pattern exists: "trench 102" then "N+ 112" then "P+ 144" then "trench 104." Moreover, this pattern is integral to the purpose of the Darwish reference in that it defines functional aspects of the Darwish device. *See, e.g.*, Darwish FIGs. 4-13 and relevant discussion including Col. 5, line 46-Col. 6, line 63. Applicant is unable to discern how such a structure could be modified in accordance with the teachings of Kocon and without undermining the purpose of the Darwish reference. More specifically, the Kocon reference does not teach nor suggest how the asserted Darwish structure could be implemented with the asserted alternating P+ and N+ regions taught by the Kocon reference. The Kocon reference teaches that the P+ and N+ regions are separated by a trench region that runs perpendicular to the intersection of the P+ and N+ regions (*i.e.*, in contradiction to the Darwish teachings there are no trench regions in the direction of and between the N+ and P+ alternating regions). Applicant notes that the Examiner appears to have overlooked this fundamental difference between the Darwish and Kocon references. Accordingly, Applicant submits that there is no teaching or suggestion that would lead one to change the fundamental structure of the Darwish reference to match the Kocon reference. Thus, Applicant submits that this proposed modification is illogical and would undermine and defeat the purpose of Darwish.

Accordingly, the rejection is improper because the prior art must evidence the motivation to implement the modification. In this instance, the Examiner alleges that the evidence is the Kocan statement of need to exploit the advantage of device size reduction. However, achieving device size reduction is in no way suggested by the Examiner's proposed modification. Moreover, by using Kocon's source/body regions (306/304 of

App. Serial No. 10/511,212  
Docket No. GB 020048US

Fig. 3C) in between the trench gates (102/104 of Fig. 11G) of Darwish, the ensuing (hypothetical) Darwish embodiment would no longer have trench gates that are accessible for signal contacts. Therefore, Applicant further submits that the §103 rejection should be removed because it lacks evidence of motivation to implement the modification.

Regarding claims 2-9, the Examiner fails to provide any evidence of motivation to modify the proposed combination of references (Darwish in view of Kocon). The Examiner acknowledges that the proposed combination does not teach the limitations of claims 2-9 and then relies upon a standard that requires that such general claim limitations be present. The relied-upon standard, as set forth in M.P.E.P. 2144.05 (citing *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)), is used to assert that "it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the cell pitch and length of source region stripes in order to have an array of cells adequately operating in a reduced space" (see, e.g., page 4, last paragraph to page 5, line 3). The Examiner's reliance upon this standard is misplaced because the admittedly-absent limitations of claims 2-9 set forth the general conditions for applying this standard. M.P.E.P. 2144.05 ("[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.").

Moreover, the M.P.E.P. indicates that such optimization arguments are applicable only where there is suggestion in the prior art to encourage such testing so as to realize the optimal modifications. In this instance, there is no evidence whatsoever that the skilled artisan would find, from the prior art, reason to experiment along the asserted paths for such optimization. In connection with this rejection, there is no such suggestion in the prior art; rather, the only motivation would appear to be improper hindsight from Applicant's Specification.

Accordingly, the Section 103(a) rejections of claims 2-9 are improper and Applicant requests that they be withdrawn.

Regarding claims 11 and 12, the Examiner fails to provide any evidence of motivation to modify the proposed combination of references (Darwish in view of Kocon). The Examiner acknowledges that the proposed combination does not teach the

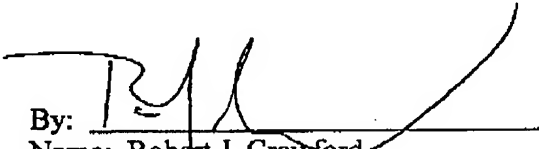
App. Serial No. 10/511,212  
Docket No. GB 020048US

limitations of claims 11 and 12 and further asserts that "it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the doping concentrations of the ruggedness regions and the source regions in order to provide a semiconductor region that can adequately conduct a current from the source to the drain" (see, e.g., page 5, lines 11-18). Once again, the Examiner simply states that one of skill in the art would be motivated to modify the proposed combination of reference without providing any actual evidence (from the references or otherwise) in support of said motivation. Moreover, Applicant cannot identify any portion of Darwish or Kocon that teach or suggest that the devices of these references do not adequately conduct a current from the source to the drain. Therefore, the Examiner's reasoning for adjusting the doping concentrations of the ruggedness and source regions is illogical. Accordingly, the Section 103(a) rejections of claims 11 and 12 are improper and Applicant requests that they be withdrawn.

In view of the above, Applicant believes that each of the Section 103 rejections has been overcome and accordingly understands that the claims should be in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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